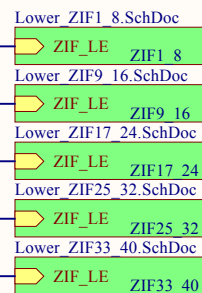
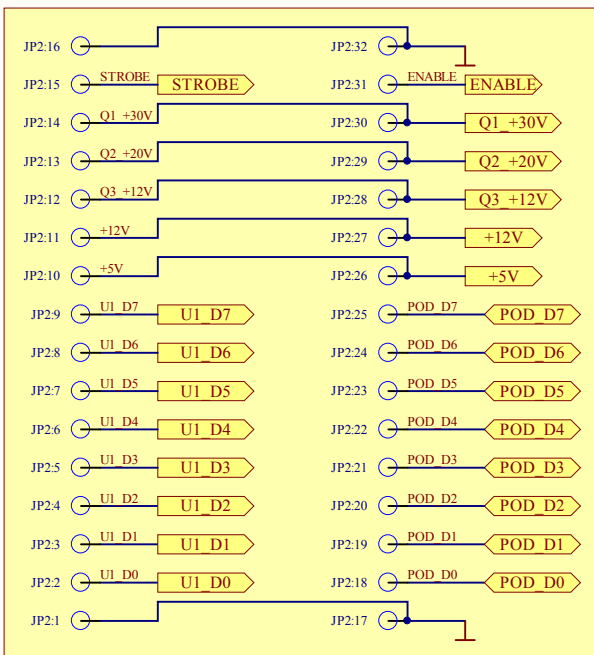
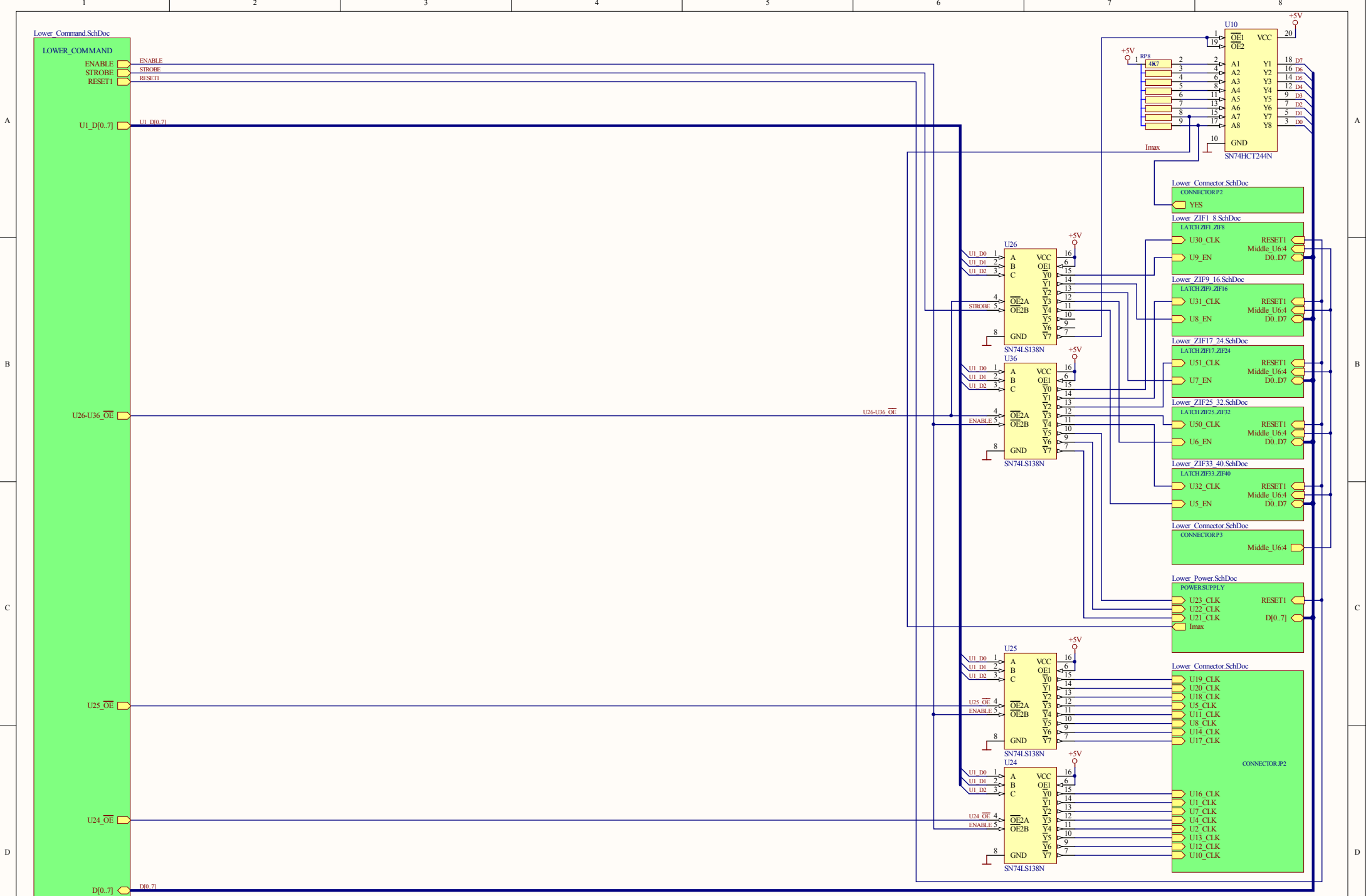


JP2

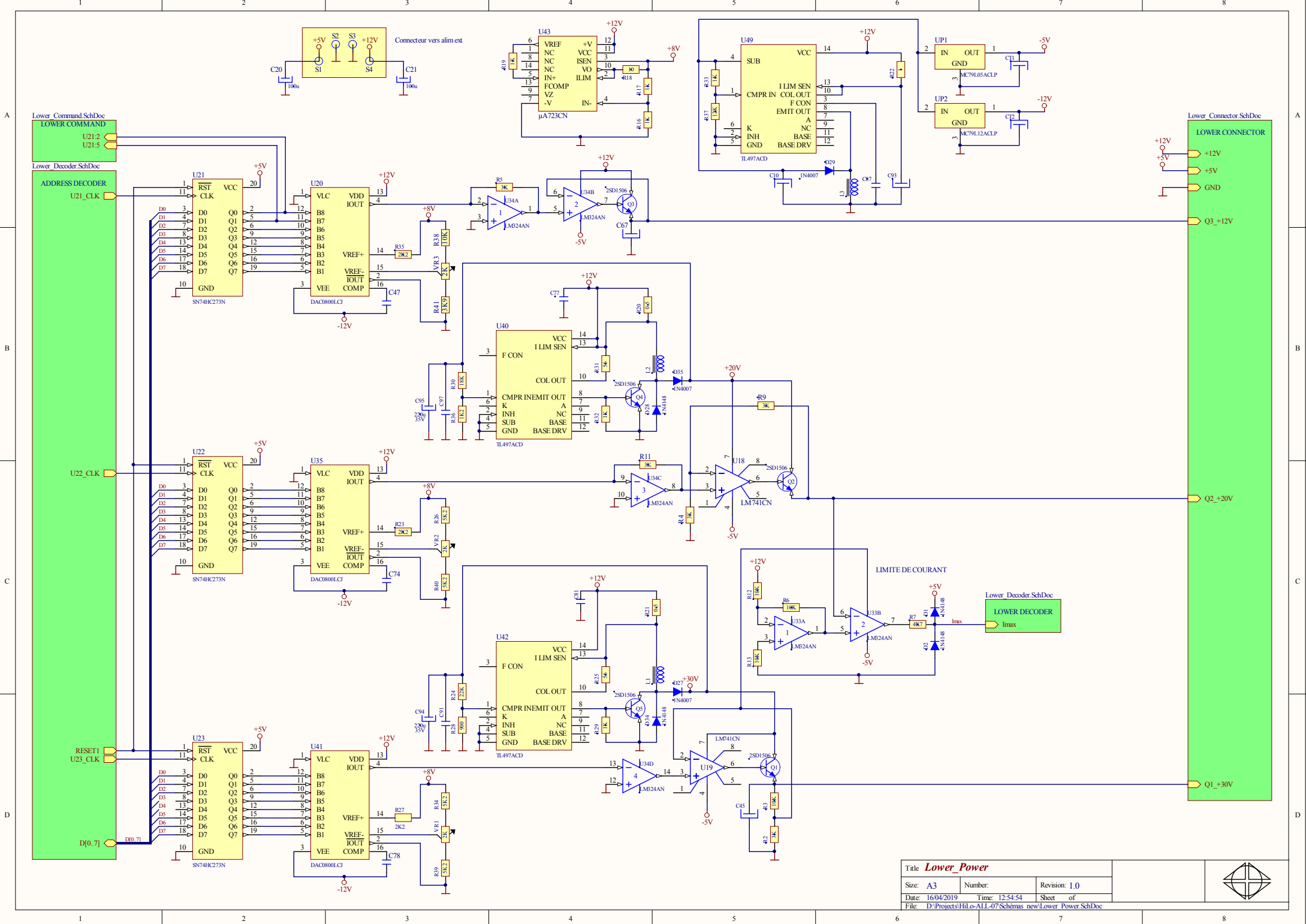


Title Lower connector			* * *	
Size: A4	Number: *	Revision: 1.0		
Date: 16/04/2019	Time: 12:53:52	Sheet* of *		
File: D:\Projects\HILo-ALL-07\Schémas new\Lower Connector.SchDoc				



Title Lower_Decoder		
Size: A3	Number:	Revision: 1.0
Date: 16/04/2019	Time: 12:54:20	Sheet of
File: D:\Projects\Hilo-ALL-07\Schemas new\Lower_Decoder.SchDoc		

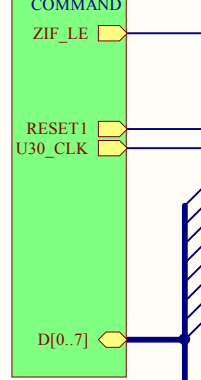




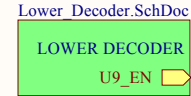
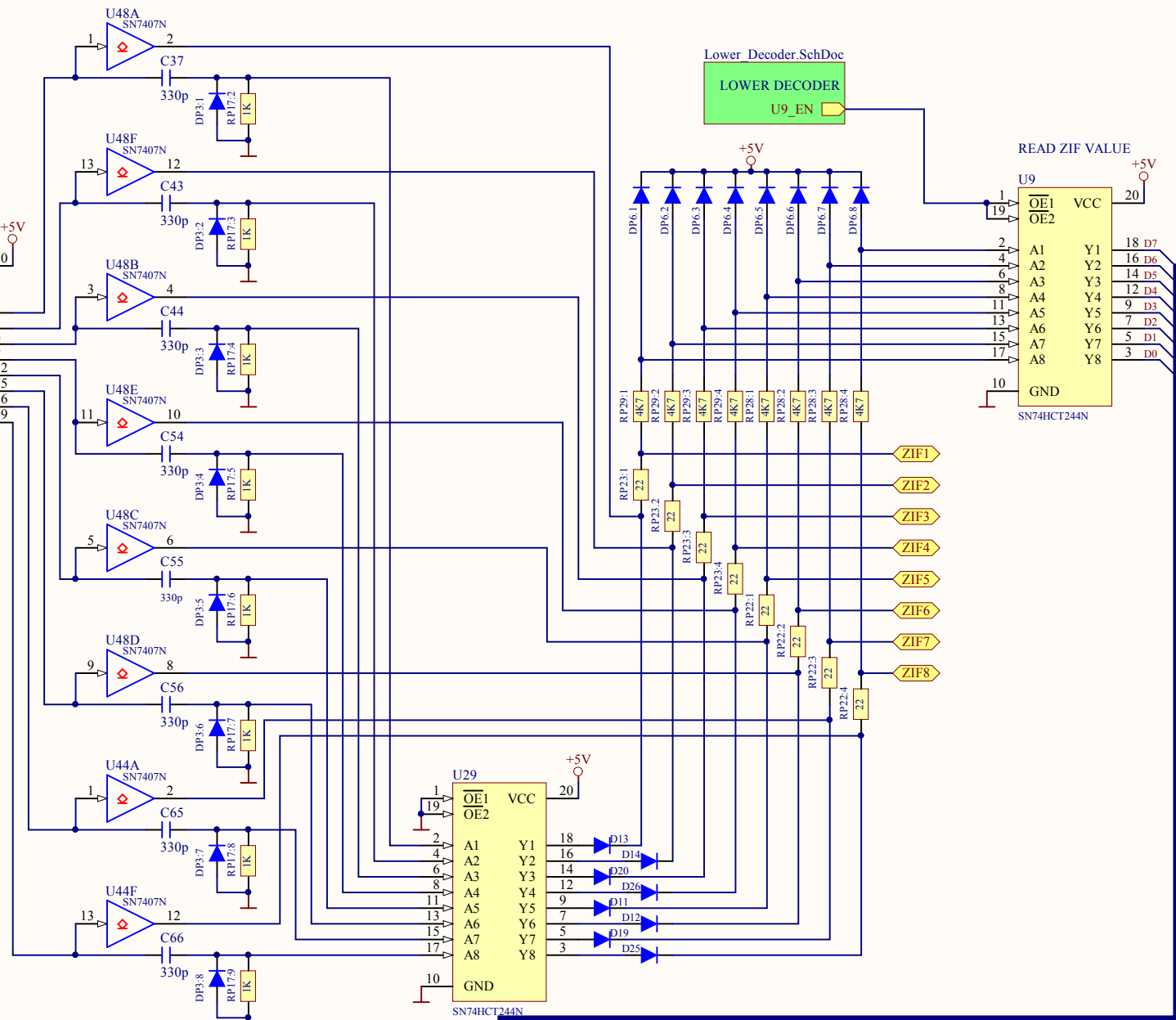
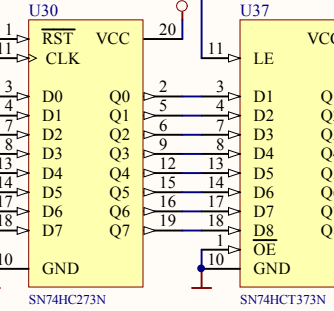
Title Lower_Power		
Size: A3	Number:	Revision: 1.0
Date: 16/04/2019	Time: 12:54:54	Sheet of
File: D:\Projects\Hilo-ALL-07\Schémas new\Lower_Power.SchDoc		



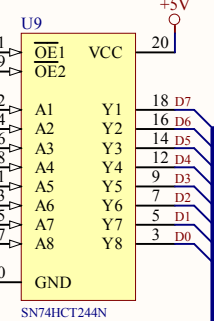
Lower_Command.SchDoc



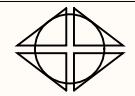
Les circuits 7407 forcent le signal ZIF à 0 volt.
 U37 low = 0V
 U37 high = high impedance



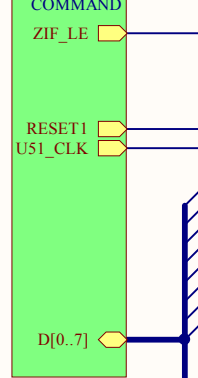
READ ZIF VALUE



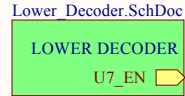
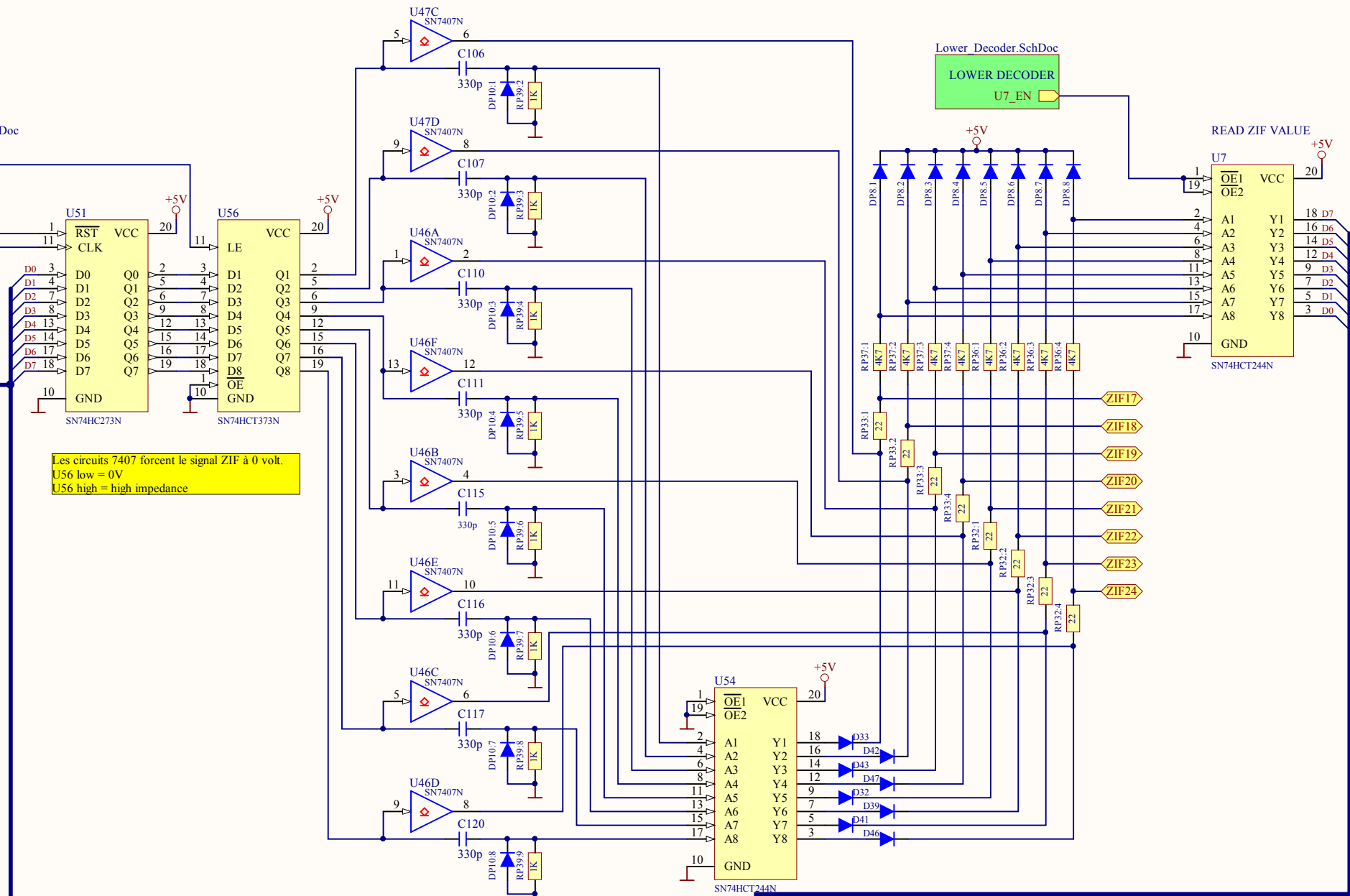
Title Lower_ZIF1-8		
Size: A4	Number: *	Revision: 1.0
Date: 16/04/2019	Time: 12:55:30	Sheet * of *
File: D:\Projects\HILo-ALL-07\Schémas new\Lower_ZIF1_8.SchDoc		



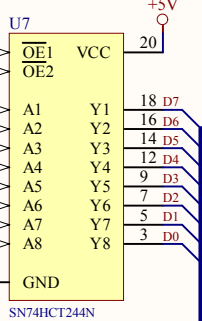
Lower_Command.SchDoc



Les circuits 7407 forcent le signal ZIF à 0 volt.
 U56 low = 0V
 U56 high = high impedance

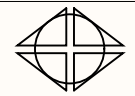


READ ZIF VALUE



- ZIF17
- ZIF18
- ZIF19
- ZIF20
- ZIF21
- ZIF22
- ZIF23
- ZIF24

Title Lower_ZIF17-24		
Size: A4	Number: *	Revision: 1.0
Date: 16/04/2019	Time: 12:55:52	Sheet* of *
File: D:\Projects\HILo-ALL-07\Schémas new\Lower_ZIF17_24.SchDoc		



Lower_Command.SchDoc

COMMAND

ZIF_LE

RESET1

U50_CLK

D[0..7]

U50 SN74HC273N

U55 SN74HCT373N

RST VCC

CLK Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8

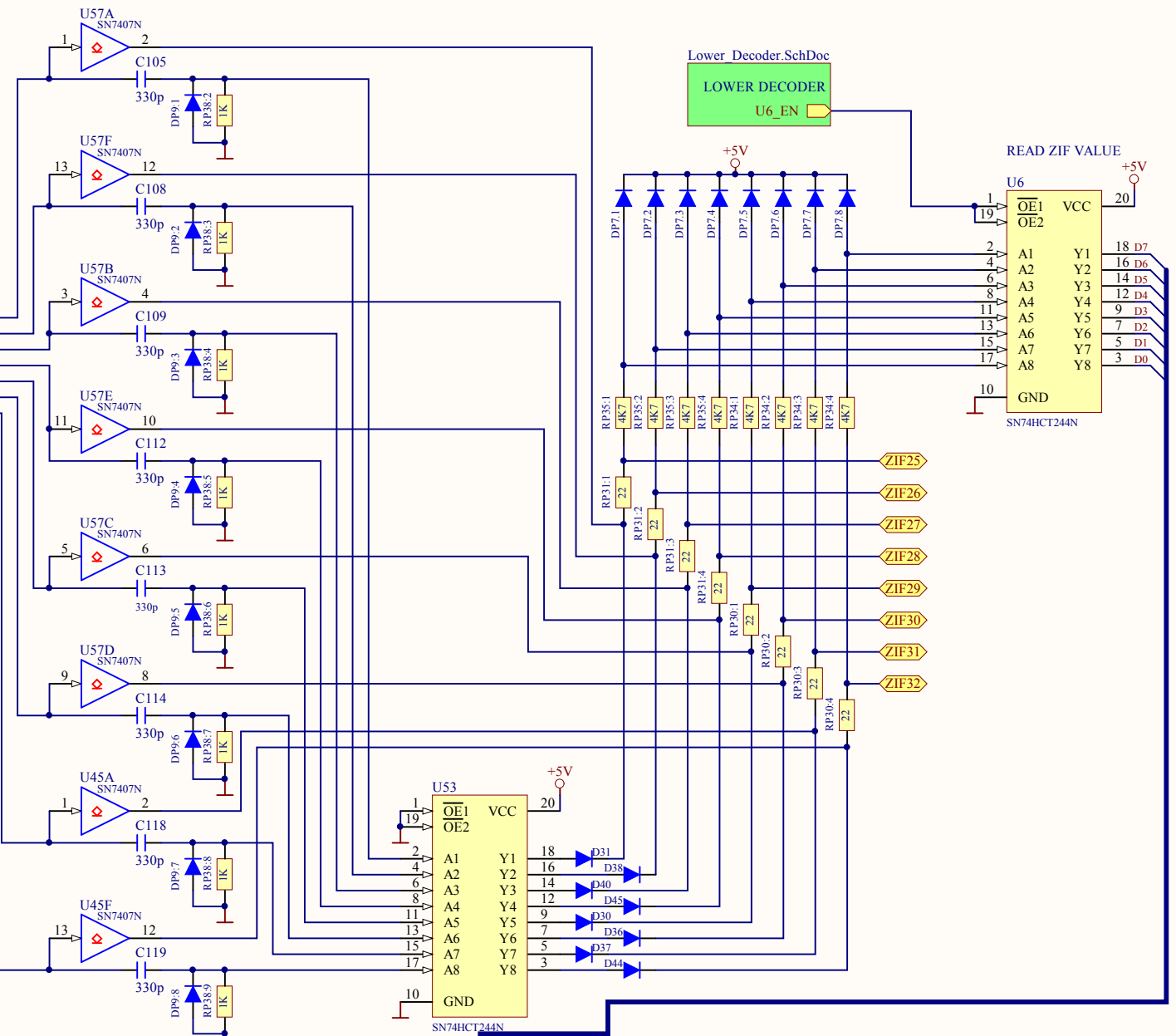
LE VCC

D0 D1 D2 D3 D4 D5 D6 D7 D8

D0 D1 D2 D3 D4 D5 D6 D7 D8

OE GND

Les circuits 7407 forcent le signal ZIF à 0 volt.
 U55 low = 0V
 U55 high = high impedance



Title Lower_ZIF25-32			*
Size: A4	Number: *	Revision: 1.0	*
Date: 16/04/2019	Time: 12:56:02	Sheet * of *	*
File: D:\Projects\HILo-ALL-07\Schémas new\Lower_ZIF25_32.SchDoc			



Lower_Command.SchDoc

COMMAND

ZIF_LE

RESET1

U32_CLK

D[0..7]

U32 SN74HC273N

U39 SN74HCT373N

RST VCC

CLK

LE

D0-Q0

D1-Q1

D2-Q2

D3-Q3

D4-Q4

D5-Q5

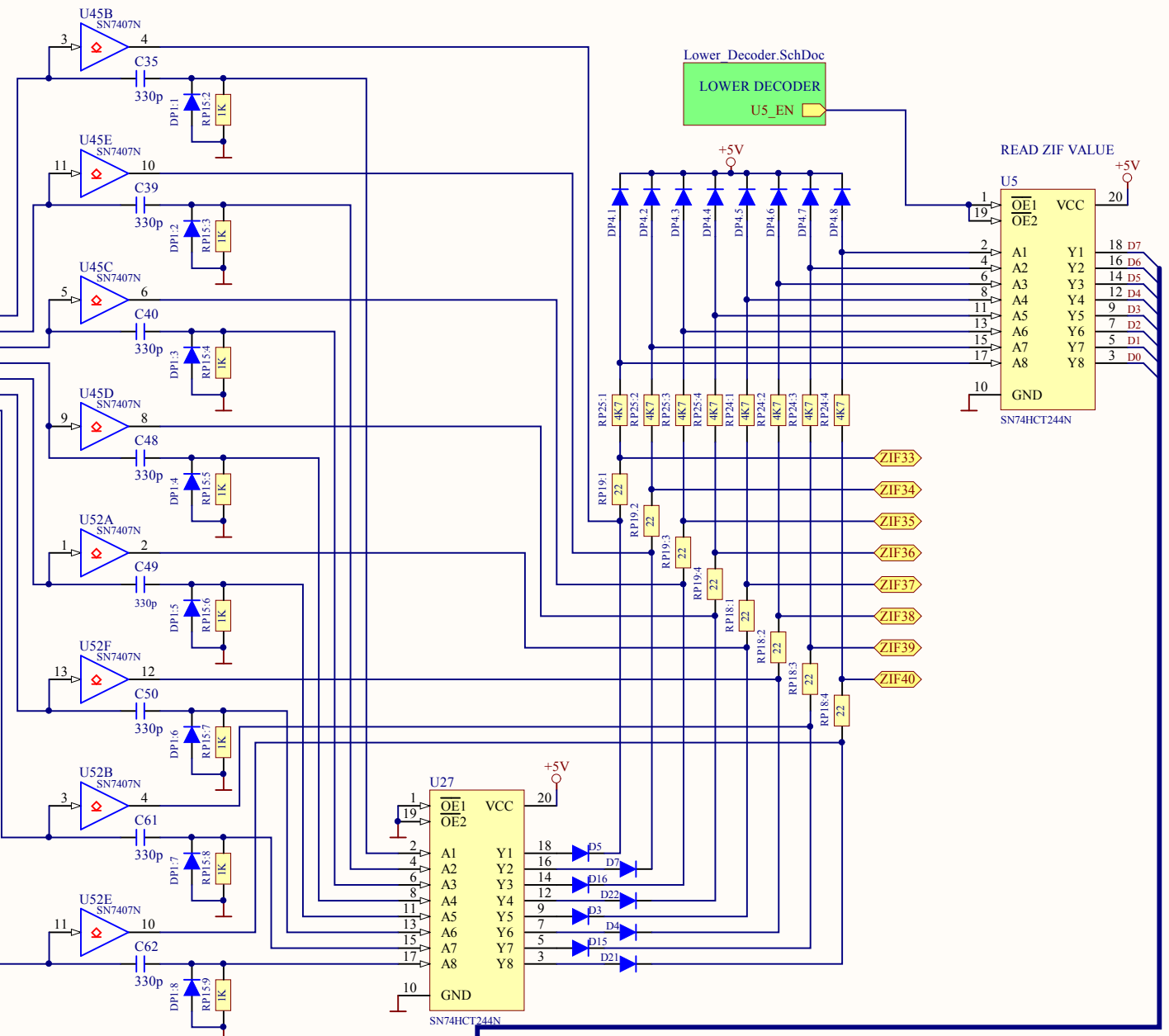
D6-Q6

D7-Q7

D8-Q8

OE

Les circuits 7407 forcent le signal ZIF à 0 volt.
 U39 low = 0V
 U39 high = high impedance



Lower_Decoder.SchDoc

LOWER DECODER

U5_EN

READ ZIF VALUE

U5 SN74HCT244N

OE1

OE2

VCC

A1-Y1

A2-Y2

A3-Y3

A4-Y4

A5-Y5

A6-Y6

A7-Y7

A8-Y8

D7

D6

D5

D4

D3

D2

D1

D0

Title Lower_ZIF33-40		
Size: A4	Number: *	Revision: 1.0
Date: 16/04/2019	Time: 12:56:12	Sheet * of *
File: D:\Projects\HILo-ALL-07\Schémas new\Lower_ZIF33_40.SchDoc		



