

# 8701 CLOCK GENERATOR

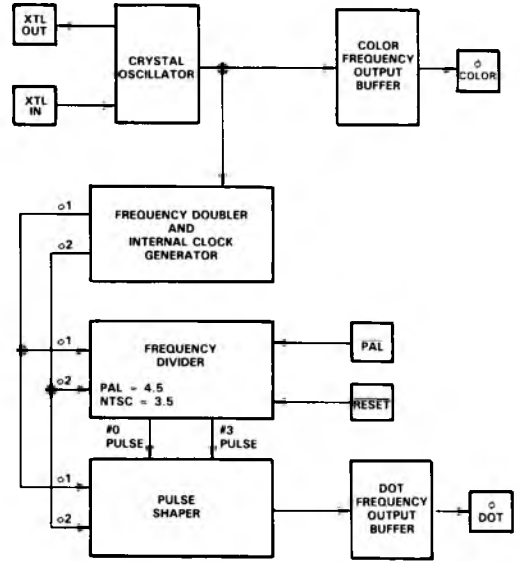
**FOLD OUT SCHEMATIC SHEET 3, PAGE 75, FOR EASY REFERENCE.**

## PIN ASSIGNMENT

N/C	1	16	N/C
VSS	2	15	VDD
N/C	3	14	XTL IN
N/C	4	13	XTL OUT
RESET	5	12	VDD
Ø DOT	6	11	N/C
PAL	7	10	N/C
Ø COLOR	8	9	VSS

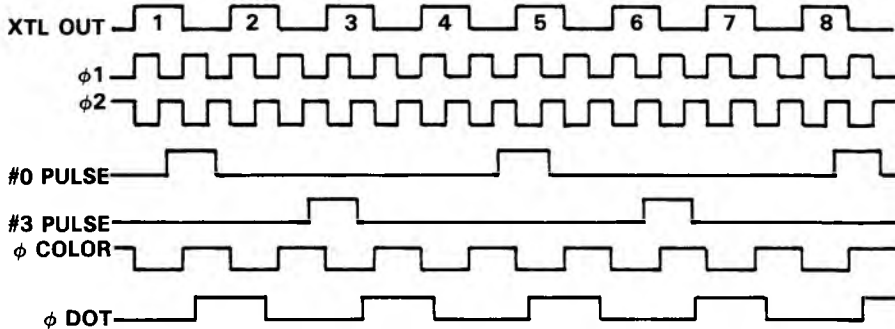
## OUTPUTS

Pin 6	Dot Clock	8.1818 MHz.
Pin 8	Color Clock	14.31818 MHz.



**Block Diagram**

The oscillator circuit uses an external crystal to generate a precise frequency, compatible with either **PAL** or **NTSC** video systems. This frequency can be fine-adjusted using an external trimmer capacitor. The output of this oscillator is buffered and becomes the color clock output. It also goes to the frequency doubler circuit. From there, a pair of non-overlapping clocks are generated (PHI1 and PHI2). These go to the frequency divider which in turn generate a pair of signals, #0 pulse and #3 pulse. Their frequency is determined by the state of the PAL/NTSC input pin. These two pulses go through some digital delays, and with the help of PHI1 and PHI2 are re-combined to form the dot clock frequency. This signal is then buffered and sent out via the dot clock pin.



**NTSC Clock Timing Diagram**