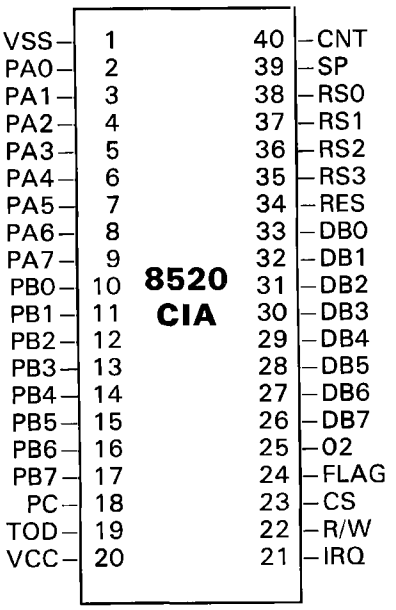
8520A COMPLEX INTERFACE ADAPTER



INTERFACE SIGNALS

02 Clock Input — The 02 clock is a TTL, compatible input used for internal device operation and as a timing reference for communicating with the system data bus.

CS — Chip Select Input — The CS input controls the activity of the 8520. A low level on CS while 02 is high causes the device to respond to signals on the R/W and address (RS) lines. A high on CS prevents these lines from controlling the 8520. The CS line is normally activated (low) at 02 by the appropriate address combination.

R/W — Read/Write Input — The R/W signal is normally supplied by the microprocessor and controls the direction of data transfers of the 8520. A high on R/W indicates a read (data transfer out of the 8520), while a low indicates a write (data transfer into the 8520).

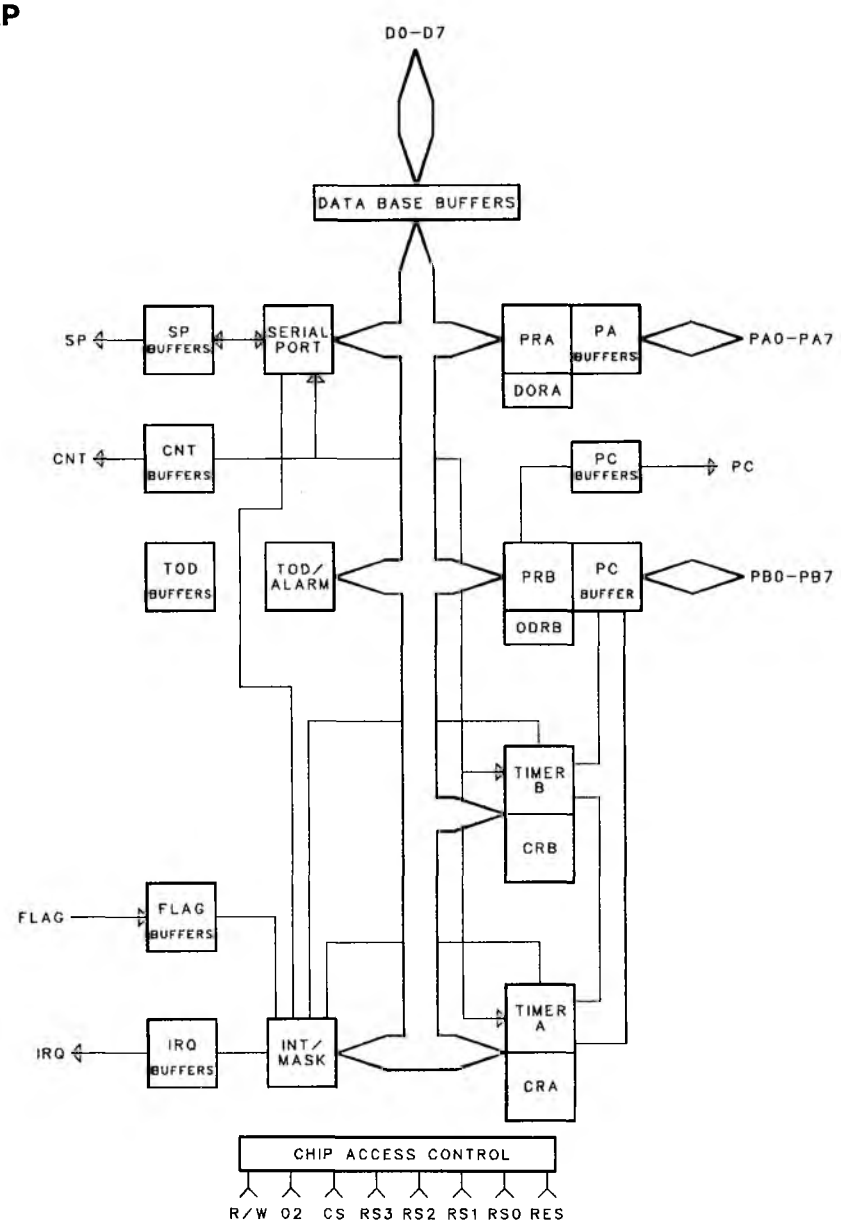
RS3-RS0 — Address Inputs — The address inputs select the internal registers as described by the Register Map.

DB7-DB0 — Data Bus Inputs/Outputs — The eight bit data bus transfers information between the 8520 and the system data bus. These pins are high impedance inputs unless CS is low and R/W and 02 are high, to read the device. During this read, the data bus output buffers are enabled, driving the data from the selected register onto the system data bus.

IRQ — Interrupt Request Output — IRQ is an open drain output normally connected to the processor interrupt input. An external pullup resistor holds the signal high, allowing multiple IRQ-outputs to be connected together. The IRQ output is normally off (high impedance) and is activated low as indicated in the functional description.

RES — Reset Input — A low on the RES pin resets all internal registers. The port pins are set as inputs and port registers to zero (although a read of the ports will return all highs because of passive pullups). The timer control registers are set to zero and the timer latches to all ones. All other registers are reset to zero.

REGISTER MAP



RS3	RS2	RS1	RS0	REG		
0	0	0	0	0	PRA	Peripheral Data Reg. A
0	0	0	1	1	PRB	Peripheral Data Reg. B
0	0	1	0	2	DDRA	Data Direction Reg. A
0	0	1	1	3	DDRB	Data Direction Reg. B
0	1	0	0	4	TA LO	Timer A Low Register
0	1	0	1	5	TA HI	Timer A High Register
0	1	1	0	6	TB LO	Timer B Low Register
0	1	1	1	7	TB HI	Timer B High Register
1	0	0	0	8		Event LSB
1	0	0	1	9		Event 8-15
1	0	1	0	A		Event MSB
1	0	1	1	B		No Connect
1	1	0	0	C	SDR	Serial Data Register
1	1	0	1	D	ICR	Interrupt Control Register
1	1	1	0	E	CRA	Control Register A
1	1	1	1	F	CRB	Control Register B